Article 2

10Gig Ethernet Signaling over Copper Backplane Interconnects

Over the past several the answers to the question of "just how fast will signaling on conventional copper backplanes go?" keeps changing. Like a similar question that used to be asked about the upper limit for baud rate on telephone modems, each attempt at an answer seems to be quickly shown to be a gross underestimate.

In a number of engineering communities, the drive to standardize and define interconnect paths at higher and higher bandwidths have also addressed the test methods and channel definition. For instance, Gigabit Ethernet and Infiniband cabling groups, not so long ago had to examine and decide on new test methods that could be used to qualify a given cable assembly for XAUI signaling at 3.125 Gb/s.

It seems almost hard to believe that a rigorous mathematical expression for differential signaling did not exist until the publication of the seminal paper "Combined Differential and Common Mode Scattering Parameters" in the July 1995 IEEE Microwave Journal. So it should not be surprising that the jury is still out deciding how to define, from a practical testing standpoint, a 10 Gb/s interconnect channel that will provide meaningful information to design engineers and silicon device engineers who might wish to specify such paths for various multi-level signaling applications.

To date, groups that have made serious attempts at such a test and characterization standard include PICMG 3.0 AdvancedTCA; Infiniband Trade Association; HPEI - SFF Committee*; HSBI - High Speed Backplane Initiative (merged with OIF); CEI - Common Electrical Interface of the OIF's PLL Committee; UXPi - IEEE ISTO; Various IEEE 802.x Committees. However, because the capabilities of semiconductors keeps advancing and the increasingly subtle nature of data errors a speeds over 3 Gb/s, these efforts cannot stop until the bandwidth limit for copper backplane interconnects is truly reached. Modems finally seemed to find their limit over POTS wiring at 56K baud.

For copper backplanes, some experts feel the upper limit will be between 20 and 40 Gb/s over a single copper path. AdvancedTCA backplanes and cards operating at 3.125 Gb/s and 6.250 Gb/s are currently being rolled out and tested at interoperability sessions. The stated goal of the PICMG aTCA specification is to offer scaleable performance to 6.25 Gb/s. Because it is generally agreed that different measurement procedures will be needed to qualify a data path at this higher rate, current standardization activities focused at data rates up to or beyond 10 Gb/s should be of particular interest.

Activity is occurring in the IEEE P-802.3ap, approved as a PAR in mid March of 2004. This working group has the stated goal of developing a standard to support 802.3 frame formats across 2 connectors over copper and FR-4 on a single pair of traces up to distances of at least one meter. This goal represents over four times the current capability of existing backplane standards such as AdvancedTCA.

DesignCon which is an annual technical convention that takes place in early February in Santa Clara has been an important venue in demonstrating methods and applications in this specialized area of signal integrity and communication system design. This past year, a new methodology called statistical eye analysis was presented to the general high performance design community. This is one of the likely analytical techniques that may be

required to implement 10 GB/s interconnect standards. Over the past several years, s-parameter techniques have emerged as the method of choice for characterizing multi-gigabit copper data channels and Stat-Eye (as it is abbreviated) combines s-parameter measurements, bit-error-rate (BER) measurements with a software based statistical algorithm to come up with a "measure of goodness" for a given backplane. Contrary to general intuition, optimizing S21 performance and selecting the best backplane for its s21 performance at the target data rate, would not necessarily yield a backplane with the best BER at that same data rate. "OK", you may say. "So it is more complicated than I can fathom." "How should an engineering group prepare for this new world of multi-gigabit signaling?"

The software tools used by backplanes and interconnect designers are more expensive than other similar software simply because the market is much smaller. To understand this fact, you must realize that for every new high-performance backplane that is designed, there are hundreds, if not thousands, of board designs that take place over the lifetime of that backplane platform. This means that while an individual company might start a new daughter card design every month, they may design a new backplane only every 3 years for that system. In standardized architectures such as cPCI, VME or the PC's PCI bus, the basic design rules for the backplane architecture once established are unchanged for years while independent companies around the world design cards for these architectures with the confidence that they will work. If you were selling backplane signal integrity software this situation would be somewhat reminiscent of the mythical bored and lonely Maytag repairman.

At the present time, it is impossible for the average hardware engineer to evaluate and choose between various available high-speed backplane connectors because the available test reports, behavioral models and evaluation boards are each based on what are oftentimes supplier specific conventions and the mechanical aspects of the various connector footprints all conspire to cloud any available data. Furthermore to collect and develop meaningful data for themselves engineers will find that the available test boards are generally inadequately documented and the sensitivity of such tests at multi-gigabit data rates are so challenging that even the most competent engineer with access to the most expensive test equipment available today, will be frustrated by the enormity of the effort. It is not that new science or technology is involved, but rather, such measurement setups are so sensitive and complex that only an engineer who spends a significant part of his professional life making such measurements is likely pull off the required experimental design and create an appropriate test fixture on the first or even second attempt.

The good news is that there existing technology that has been developed within a different industry that is available and waiting for use by backplane designers. This industry is the microwave test and measurement community. It turns out that the analytical tools, field solvers and test equipment is now being discovered as the right solution for the backplane design industry. One technical issue that remains is to solve the particular requirements specific to the mechanical characteristics of the connector interface and contact assemblies.

Another challenge is for the industry to come to agreement about how the data will be collected and presented so that it will be immediately useful to all engineers who must be involved in the process. The ideal solution would be one that is a result of a collaborative industry wide effort. The various segments that should be involved are the semiconductor vendors, test equipment manufacturers, analytical software vendors as well as 3D mechanical geometry software tool vendors and specialized field solver developers. The hardware OEMs, the signal integrity design consultants and academics all would have valuable input. Examples of such existing collaborations are the IBIS user community, the OIF CEI initiative, and the IEEE Journal of microwave theory and methods.

It is not enough to have the right data, it needs to be in a form that makes it usable for evaluation, to support hardware design and also to support test debug activities. The form and availability of the data must be familiar to engineers so that they will already under the context and assumptions inherent in the data supplied. There might be a rev 1 methodology for 2 -5 Gb/s, a rev 2 methodology for 3 - 10 Gb/s applications and a rev 2

methodology for 6- 15 Gb/s applications. Such an approach would define, characteristic data types, test setups, test fixtures including equipment tolerances, PCB laminate materials, contact geometries and cabling, as well as software transformations and data structures.

Right now is the time to begin these activities. Maybe the newly formed IEEE P-802.3ap will take us further down the path already started by Infiniband, Gigabit Ethernet, HSBI, CEI, UXPi and AdvancedTCA. As stated in the 802.3ap objectives, "The proposed specification will use copper media similar to other high speed networking technologies but does so with the IEEE 802.3 MAC as the over-riding layer which will result in higher compatibility and lower cost for Ethernet systems." As a further statement supporting the broad market appeal, the 802.3ap objectives included the comment, "156 participants attended the Ethernet Over Backplane call-for-interest, representing at least 33 companies, and indicated that they plan to participate in the standardization of Ethernet Over Backplane. This level of commitment indicates that a standard will be developed by a large group of vendors and users."

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*P802.3ap - Information technology -- Telecommunications and information exchange between systems -- Local and metropolitan area networks -- specific requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Amendment: Ethernet Operation Over Electrical Backplanes.