The Bus Architecture Cheat Sheet

based on earlier material developed
by Michael Thompson.

VME Systems

VME IEEE-1014
2 piece pin and socket connector (DIN 41612, IEC 603-2)
3U x 160mm, 6U x 160mm card sizes
J1 backplane: 16 bits data, 24 bits address
J1+J2 backplane: 32 bits data, 32 bits address
Asynchronous protocol
35 megabytes/second bandwidth VME 64 to 80 megabytes/second

The VME (VERSAmodule Europe) bus was introduced by Motorola-Europe in 1980 as two-piece-connector, eurocard version of Motorola's VERSAbus. The VERSAbus was designed well, but did not sell well in Europe because of its card-edge connector. Motorola, Mostek, and Signetics brought the VME system to the U.S., and eventually IEEE standardized it. The VME bus was originally a 16 bit bus like its predecessor, the Versabus. A system with a 16 bit VME bus uses only the J1 backplane. This allows a system to be built with only 3U height boards. The system bus can be expanded to a full 32 bits by the addition of a second backplane, the J2. The J2 backplane also provides additional +5V and ground connections for 6U height boards.

Since the maximum bandwidth of a VME bus is limited to about 35MHz, the performance of the next generation of VME systems will be limited by the bus. The VME International Trade Association (VITA) has proposed VME64 which multiplexes the address and data lines and with the use os SSBLT (source synchronous block l?? transfers) will allow data rates of 80 megabytes/second. For a next generation architecture VITA has adopted Futurebus+ which has a bandwidth of about 100 MHz and is expandable from 32 bits to 128 bits with various approved profiles. This should be sufficient until optical busses are available.

VMX / VSB IEEE-1096
2 piece pin and socket connector (DIN 41612, IEC 603-2)
40 megabytes/second bandwidth

When multiple CPUs share the same VME bus, there are conflicts which limit the performance of the system. To improve the performance of the VME system, private processor-to-memory buses can be added. The private buses provide a means for the processor to access memory without having to use the VME bus. The private buses allow multiple processors to run concurrently on multiple VSB buses in a VME system, without interfering with each other. The VMX and VSB backplanes are limited to 6 slots in length, and plug onto the tails of the unused pins of the VME J2 backplane.

VMX is rapidly being phased out in favor of the more capable VSB bus, which was introduced in 1986.

VMS IEEE-1132
3.2 megabytes/second bandwidth

VMS is a serial bus that uses two of the pins on the J1 backplane. This low performance bus can be used for simple interfaces like a printer port or a floppy disk controller. The VMS bus has yet to receive much utilization.

Sun Microsystems
9U x 400mm card size

Sun Microsystems, with over $1,000,000,000 in annual sales, is one of the world's largest producers of engineering work stations. Sun used Multibus-I for their Sun 2 work stations but switched to VME for their newer and higher performance Sun 3s and Sun RISC 4s. In addition to the standard VME bus, Sun has a proprietary bus, which is similar to VSB, and uses the uncommitted pins of the J2 backplane, and a proprietary J3 backplane. Because of the large board size, extra power is brought into the system via the J3 backplane. Sun currently offers 3, 6, and 12 slot work stations. The Sun 12 slot tower has limited cooling capacity and only a 735 Watt power supply. Mupac is producing a 14 slot tower for a Sun OEM which addresses these limitations.

VXI IEEE-1155
3U x 160mm, 6U x 160mm, 6U x 340mm, 9U x 340mm card sizes
2 piece pin and socket connector (DIN 41612, IEC 603-2)
Made up of VME J1+J2 with optional J3
Asynchronous protocol
100 megabytes/second bandwidth

VXI was introduced in 1987 as an extension of the VME bus, specifically for instrument-on-a-card applications (IAC). The first supporters of the bus were Colorado Data Systems, Hewlett-Packard, Racal-Dana, Tektronix, and Wavetec. Recently Bruel & Kjaer, National Instruments, Fluke, Keithley, and Genrad have joined the VXIbus consortium.

The VXI bus uses the VME bus as the main bus, but adds analog power pins, a local bus, a 10MHz ECL clock, ECL and TTL trigger signals, and module IDs to the P2 connector. The optional P3 backplane adds the same signals as the P2 but at a much higher performance level. The ECL clock on the P3 runs at 100MHz. Using the P3 backplane, data rates in excess of 100 Mbytes/second are possible. The VXI specification includes larger boards than the VME standard, allowing the use of boards up to 9U x 340mm. The VXI specification also allows for 1.2" wide modules instead of the standard .8" width. This larger spacing leaves room for shielding around plug in modules. The U.S. Air Force has adopted VXI as the basis for the MATE-STD-IAC standard. All new modular automatic test equipment for the Air Force will use VXI. Colorado Data Systems has several VXI products on the market that meet military requirements.

The VME market has experienced phenomenal growth. The adoption of VME as the core bus for Sun and VXI systems just increases an already large market.

There are over 300 manufacturers sharing about $375,000,000 in VME business (not including Sun). Motorola has the largest share with about $80,000,000. The total VME market is projected by VITA to reach over $1,000,000,000 by 1995.

Multibus Systems

Multibus-I IEEE-796
86+60 contact card edge connectors
7" x 12" card size
16 bits data, 24 bits address
Asynchronous protocol
4 megabytes/second bandwidth

Multibus-I was introduced by Intel in 1976, making it one of the first bus specifications. It was originally designed for 8 bit CPUs, but it was later expanded for the 16 bit 8086 CPU. The bus was expanded again to add

four more address lines in order to fully utilize larger memory capacity of the 80286 CPU. The four additional address lines are on the P2 connector.

LBX
60 contact card edge connector

To improve the performance of Multibus-I systems, private processor-to-memory buses can be added. The LBX bus is a private bus that uses the remainder of the pins on the P2 connector.

The Multibus-I bus was specifically designed for the OEM market. The major markets are commercial and industrial. Even though 32 bit CPUs will run on MB-I, performance of the system is backplane limited because of the 16 bit data path. There is an ongoing effort by Zendez to get the bus standard extended to full 32 bits.

There are over 135 manufacturers sharing $XXX,000,000 of MB-I business. Intel has the largest share at $XX,000,000.

MULTIBUS-II IEEE-1296

PSB
2 piece pin and socket connector (DIN 41612, IEC 603-2)
6U x 220mm card size
32 bits data, 32 bits address
Synchronous protocol
40 megabytes/second bandwidth

MB-II was introduced by Intel in 1983 as a 32 bit follow-on to Multibus-I. The mechanical packaging of MB-II is based on the eurocard because of the reliability problems of MB-I's card edge connector. The Multibus-II bus architecture is broken up into four parts, memory, I/O interconnect, and message. All of these access methods are physically implemented on the parallel system bus, the PSB. Message passing provides the main connection between boards plugged into the Multibus-II backplane. A bus interface chip called the MPC, message passing co-processor, sends and receives messages between boards in the system. All references to I/O or memory go through the MPC. Multibus-II systems do not have interrupt lines, like most systems, for a peripheral to indicate to the processor that it needs service. On most computer systems, the peripheral signals

the processor via an interrupt line on the backplane, and then the processor reads the information from the peripheral controller board. On a MB-II system, the peripheral sends an unsolicited message via the MPC to the processor. This message contains all of the information needed for the processor to service the peripheral, saving many bus cycles and time. The message passing co-processor is capable of transferring information across the MB-II backplane much faster than the CPU. The MPC automatically retries transfers when it detects bus errors improving the reliability of the system. The MPC helps the CPU to do its job, improving the performance of the system. Interconnect Space is an address that is based on the backplane slot that a board is plugged into. This allows the CPU to access registers on a board in order to determine what the board is, who manufactured it, and how to configure the board and the software to use it.

This technique allows boards to be designed without configuration dip switches, greatly simplifying field service and upgrades. Most MB-II boards use an microcontroller to run the MPC. The use of the microcontroller allows for built in self test, BIST. When the system is powered on, all of the boards test themselves, and the CPU can see if all the boards are operational by reading a register in the boards interconnect space. Address Space and I/O Space are just like conventional memory and I/O on any other computer.

LBX-II
2 piece pin and socket connector (DIN 41612, IEC 603-2)
High speed memory to CPU bus for J2
48 megabytes/second bandwidth

MB-II has a private processor to memory bus, the local bus extension or LBX-II, which performs just like BLX on a MB-I system, but has Interconnect Space as well as Memory Space.

SSB
CSMA/CD serial bus on PSBS backplane
175 kilobytes/second bandwidth

The SSB is a low performance serial bus that uses two pins on the PSB backplane. The SSB is intended for slow peripherals like printers and floppy disks. The SSB has not been used widely yet.

Bitbus
CSMA/CD serial bus

The SSB is a low performance, low cost bus on two pins of the PSB backplane. The SSB looks just like a small local area network. The SSB can also be used to interconnect multiple MB-II systems through a connector on the LBX-II backplane.

Mupac built the first MB-II products ever sold, a 6 and 9 position backplane/cardcage and a wire-wrap board. These were used to prototype the first MB-II products produced by Intel. MB-II has had a much slower growth than Intel planned on, mostly due to the complexity of the bus interface, and an initial lack of silicon bus interface support. Large OEMs like Prime and GE have adopted MB-II, therefore the rate of market growth should increase.

There are more than 75 manufacturers sharing about

$XX,000,000 on MB-II business. Intel has the largest share at $X,000,000.

IBM-PC/AT/PS2 IEEE-996

IBM-PC
62 contact card edge connector
3.9" x 13.2" card size
8 bits data, 20 bits address

IBM-AT/ISA IEEE 996

62 + 36 contact card edge connector
5.25" x 13.2" card size
16 bits data, 24 bits address
4 megabytes/second bandwidth

The IBM PC-AT was introduced in 1985. This bus is generally considered the most popular bus. It is a low cost, low performance bus, and no one company controls the bus specification. Industrial versions of the PC-XT and PC-AT are available from IBM.

There are over 150 companies sharing $X,XXX,000,000 of IBM-PC add-in board business.

In 1991 a consortium was formed to maintain the standard when IBM introduced the PS2 Microchannel architecture. The classic architecture was named the Industry Standard Architecture (ISA).

IBM-PS2 Microchannel

IBM-PS2
?? contact card edge connector
3.46" x 11.5" card size
32 bits data, 32 bits address
8 megabytes/second bandwidth

The IBM PS2 was introduce in 1987. Only advanced when compared to IBM-AT. Has a well published specification, but has undefined royalty and patent issues. It incorporates self-configuration features which are similar to Futurebus and MB-II. It still uses a card edge connector instead of more reliable two piece connectors.

EISA Bus

This is the ISA answer to the IBM microchannel. It is a high

performance 32 bit bus which allows backward compatibility with PC/AT/ISA designs through the use of an innovative connector design developed by Burndy. The form factor is the same as PC/AT/ISA. Standard PC/AT/ISA boards can plug into this bus and communicate over a 16 bit wide data path. This design is expected to be competitive with VME on a electrical performance basis but is handicapped by the less robust PC style mechanical structure and edgecard connector technology.

NuBus IEEE-1196

2 piece pin and socket connector (DIN 41612, IEC 603-2)
9U x 280mm card size
32 bits data, 32 bits address
Synchronous protocol
40 megabytes/second bandwidth

The NuBus was originally developed at MIT in 1979. The rights were then sold to Western Digital in 1983. The NuBus was the first bus to have geographic addressing, allowing a self-configuring computer system. Westen Digital's NuBus group was sold to Texas Instruments. TI's Lisp machine, made for the artificial intelligence market, is based on Western Digital's work, and uses the NuBus. The NuBus was recently adopted for the Apple Mac-II. Apple's use of the NuBus is causing the development of a large number of I/O boards, and may cause an increase in the use of the larger 9U x 280 size of NuBus boards. However card and format size does not conform to eurocard.

There were at one time over 15 companies sharing $33,000,000 of NuBus add-in board business. Apple had the largest share with $10,000,000 in sales.

Futurebus IEEE-896

2 piece pin and socket connector (IEEE 1301.1, IEC)
12Ux 12U card size (approximately 300mm x 300mm)
32 bits data, 32 bit address, is defined to 128 bits
30 mm card spacing
Asynchronous protocol
100 megabytes/second bandwidth at 32 bits
400 megabytes/second bandwidth at 128 bits

The Futurebus was first introduced in 1987 by the IEEE after 9 years of development. Later it was changed significantly to require a "hard" metric mechanical structure and provide for central arbitration. Further changes involved the development of various "profiles" which represent various combinations of features such as bus width, card size, arbitration method, I/O pin outs, and available voltages.

This was the first bus standard not designed and controlled by a single corporation. This bus uses BTL (backplane transceiver logic) drivers instead of the usual TTL drivers. The BTL transceivers have only a IV swing and generate trapezoidal waveforms. The controlled rise and fall times of the signals also allow the receivers to incorporate digital noise filters. There are Schottky diodes in the receiver chips which dramatically decrease the capacitive loading on the backplane. This reduces the changes in backplane characteristic impedance as more boards are plugged into the

backplane. The resulting small impedance change allows the backplane terminator to perform better. This bus has the capability of being expanded to 128 bits of address and data, which make it the highest performance bus available.

Currently a number of manufacturers offer CPU cards based on the 64 bit data width of profile A and F. The complex data transfer protocols and multiple profiles have been a significant impediment to broad acceptance of the architecture. Currently both Texas Instruments and NewBridge Microsystems offer complete interface chip sets.

Profiles either currently defined or in working group are:

A IEEE 896.2 Most popular
B IEEE 896.2 I/O bus?
F IEEE 896.2 Popular interface but 128 bit not used
M IEEE 896.5 Military includes 12SU 10SU and SEM E
T IEEE P896.6 Telecom
C IEEE P896.7 Interconnection fabric- embryonic
D IEEE P896.8 Desk top -still in transition
S IEEE P896.10 Space- not conventional BTL

G-64/G-96

G-64
2 piece pin and socket connector (DIN 41612, IEC 603-2)
3U x 160mm, 6U x 160mm
16 bits data, 16 bits address
2 megabytes/second bandwidth

The G-64 bus was introduced by Gespac in 1979 as a low cost bus system for the industrial market. Gespac was formed by a group of former Motorola-Europe employees. The G-64 bus can be used as an intelligent I/O subsystem for a VME system.

G-96
2 piece pin and socket connector (DIN 41612, IEC 603-2)
16 bits data, 24 bits address
10 megabytes/second bandwidth

The G-96 bus is a 32 bit version of the G-64. The G-96 was introduced in 1984. The G-96 has 16 times the memory space of the G-64 bus, and higher performance.
The bus is extremely popular in Europe but has seen little use in he U.S. There were at one time 15 manufacturers, including Thomson Semiconductor and Fujitsu, producing 400 different boards, and sharing a $XX,000,000 market. Gespac boards have been second sourced by Thomson since 1980.

S-100 IEEE-696

100 contact card edge connector
5.125" x 9.925" card size
16 bits data, 24 bits address
4 megabytes/second bandwidth

The S-100 bus was introduced by MITS in 1975, and was based on the pin out of the 8080 CPU chip. The name came from the 100 contacts on the bus connector. It has low

bandwidth, card edge connectors, and unregulated backplane voltage sources, which have limited its potential.

The bus was extremely popular in the late '70s and early '80s but now is generally considered a dying market. There were more than 75 companies sharing $XX,000,000 of S-100 business. Cromemco had the largest market share at $XX,000,000.

STD-Bus IEEE-961

56 contact card edge connector
4.5" x 6 card size
16 bits data, 20 bits address
8 megabytes/second bandwidth

The STD was introduced to the market by Pro-Log in 1978. The bus was originally designed as an 8 bit, low cost system for the industrial market to replace discrete logic controllers. The bus was expanded to 16 bits in the early '80s. The small board size does not allow much functionality on a single board, therefore there is an incredible number and variety of boards available. There are over 25 different CPU chips that are available on boards for the STD bus, including 32 bit CPUs like the 80386. One of the most important developments for this bus is a STD bus system that runs MS-DOS and is software compatible with the IMB-PC. The bus has been expanded to 16 bits to use the newer, high performance CPUs on the market. The STD bus specification was recently expanded to include CMOS boards. This allows STD bus products to easily be run from batteries and operate in a temperature range of -40C to 85C. The card edge connector is the biggest detriment to system reliability and may cause any new designs to be based on STE, the eurocard version of STD. Most bus survey show this bus as the most popular next to IBM-PC-AT.

There were over 150 companies sharing $XXX,000,000 in STD bus business.

Pro-Log had the largest share at $XX,000,000. There are more than 1,000 different boards produced for the STD bus.

STE Bus IEEE-1000

2 piece pin and socket connector (DIN 41612, IEC 603-2)
3U x 160mm card size
16 bits data, 20 bits address
5 megabytes/second bandwidth

The STE bus, introduced in 1986, is the STD bus built on a eurocard format. The card edge connector was a reliability limitation on the STD bus which was replaced with a DIN connector on the STE bus.

There is little market for STE boards at this time.

Digital Equipment Buses

UNIBUS
6 36 contact card edge connectors
16 bits data, 22 bits address

1 megabytes/second bandwidth

The Unibus was the first 16 bit bus designed by DEC, and was introduced in the early '70s. The PDP-11 systems were originally all based on the unibus. The bus has 6 connectors per slot, but allows the use of 4 and 6 connector boards. The first model of the VAX, the VAX 11-780, used the Unibus as its I/O bus. This design allowed all of the I/O boards from PDP-11s to be used on the new VAX.

There are over 80 companies sharing $XX,000,000 of UNIBUS business. Digital Equipment has the largest share with $XX,000,000 in sales.

Q-Bus
4 36 contact card edge connectors
16 bits data, 22 bits address
3.3 megabytes/second bandwidth
12.9 megabytes/second bandwidth with PMI

The Q-bus was introduced by Digital Equipment in 1974. The bus was designed as a low cost, lower performance, alternative to the Unibus. The new MicroVAX-IIs use the Q-bus, as does the PDP-11/83, because there is no longer a need for the larger board size of the Unibus. The current revision of the Q-bus also implements a Private-Memory-interconnect (PMI) bus that provides a private bus between the CPU and memory boards. The PMI bus has only address and control signals. All data transfers till take place on the Q-bus. The lack of handshaking on the PMI bus quadruples the memory transfer rate of the Q-bus. The Q-bus still has potential to evolve and retain market share.

There are over 115 companies sharing $XXX,000,000 of Q-bus business. Digital Equipment has the largest share with $XXX,000,000 in sales.

VAX-BI bus
4 ?? contact ZIF card edge connectors
11.7" x 11.7" card size
32 bits data, 32 bits address
14 megabytes/second bandwidth

The VAX-BI (Bus Interconnect) bus, introduced in 1982, is used in Dec's high end VAX systems. Dec has extremely tight control of the patents on BI and the licenses to use the BI architecture. The bus is complex and requires a special interface chip only available from DEC, 12 layer boards, and expensive ZIF connectors. Even with the new technology incorporated in the design the bus has less performance than MB-II and VME systems.

Fastbus IEEE-960

2 piece, four row, pin and socket connectors IEEE 1301.1
Hard Metric IEEE 1301
200 megabytes/second bandwidth

The Fastbus was introduced in 1984 by the U.S. Department of Energy and ESONE. The mechanical packaging standard was IEEE-583 CAMAC. The bus specification was later turned over to IEEE. Around 1993 it was redefined based on some of the concepts developed in IEEE 896.1. In its earlier

version it was the most popular bus for use in physics research due to it's extremely high bandwidth. The jury is still out on the revised version. The bus use 10K ECL logic to drive the backplane instead of the more usual TTL.

This allows for high switching speeds but has a severe power consumption penalty. There are even provisions for water cooling the card cages which allows up to 3000W per card cage. The Fastbus also has provisions for interconnecting multiple backplanes together as one system, allowing for a maximum of 4,278,190,080 boards per system.

The size of the Fastbus market is difficult to determine because most of the purchases are on-time-only for a particular research project.

Rugged Bus IEEE P1496 (obsolete)

The Rugged Bus was an effort to design a standard bus for harsh environment applications. The standard was originally under the control of SAE but then turned over to IEEE where many of its concepts were incorporated into the various environmental of Futurebus. The par was later withdrawn.

Mechanical and Connector Standards

IEEE-1101 The Standard Eurocard Mechanical Format

Since the mechanical standards that all eurocard systems are based on are in several difficult to comprehend documents, the IEEE wrote their own mechanical standard. This standard is based on the following specifications: IEC-297-1 mechanical structures, IEC-297-2 front panels, IEC-297-3 subracks and plug-in units, IEC-603-2 connectors, and EIA-RS-310 front panels. The IEC-603-2 connector specification is an international version of the DIN-41612 German connector specification. This document puts all of the information required to build mechanically compatible eurocard systems in one document. All IEEE bus specifications that are eurocard compatible reference this document for mechanical standards.

IEEE-1101.3 Mechanical Std. Conduction Cooled Eurocards

Since many military programs require conduction cooling this standard was developed to allow the various VME manufacturers to standardize on mechanical format for conduction cooled applications.

IEEE-1101.4 SEM E Standard Electronic Module (Military)

This format was to provide a rugged format for Military Futurebus+ applications. It utilizes a 396 pin, eight row, blade and fork closed entry connector design. The connector

is currently offered by Cannon, Teradyne and CTS.

PIEEE-1101.5 SEM E Mech. Std. for Air Flow Thru Modules

This specification is still under development and is sponsored by Hughes Aircraft.

PIEEE-1101.6 10SU Mech. Std. for Air Flow Thru Modules

This specification is still under development and is sponsored by Hughes Aircraft.

PIEEE-1101.7 SEM E Stretch Mech. Std. for Military Mods.

This specification is similar to the SEM E design but was needed to provide a greater board area deemed necessary for many space applications that did not have quite the severe environmental requirements for which the original SEM E was designed. It is currently being sponsored by the National Research Laboratory.

IEEE-1301 Hard Metric Mechanical Practices

This is the "hard" metric standard developed for Futurebus+ and originally sponsored by Hans Carlson of Erickson. All dimensions are to be multiples of 2.5mm, 5mm, and 25mm. All screws are to be metric. This system is part of a comprehensive standard that includes plug in cards, plug in modules, backplanes, subracks, enclosures, equipment racks and computer room floor and wall dimensions. EIA 810 version D takes into account the old EIA 810 C equipment rack designs as well as the requirements of IEEE 1301 and recommends coordinated flange designs.

IEEE-1301.1 Hard Metric Connector Mechanicals (Metral)

This standard was developed for IEEE 896.2 Futurebus+ hard metric profiles. Originally proposed by David Brearly of DuPont, compliant connectors are now produced by Berg, Erickson, AT&T, CECO, Cannon, Custom Stamping, Sorieu/Burndy, AMP and others. It was proposed as an inexpensive (>2.5 cents/pin) high density connector with sufficient electrical characteristics to support BTL incident wave designs. These were the perceived needs of the telecommunication industry which was the early supporter of Futurbus. The connector supports keying, extended pins for live insertion schemes, various coaxial designs, both 1 amp signal pins and wider 2 amp power blades. It is a four row 2mm x 2mm design with the male connector on the backplane and the female in a right angle or tandem tail design. Most common formats are offered in pressfit thru hole designs.
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