Memorandum

To: *Bob Rozell*
From: *Mike Munroe*
Date: *16 March 95*
Subject: *PCI Peripheral Component Interconnect*

At the present time the PCI local bus is growing at a tremendous pace. It started in the personal computer industry, as a processor local bus to support add-in graphics processor boards. The original chip set was developed by Intel. In this application, it has displaced several previous video bus architectures such as VL bus. Today the large and growing number of PCI based peripherals has caused the PCI architecture to be incorporated into a number of commercial applications. The IEEE 1386 committee under the influence of DEC, Molex and Berg completed a mechanical form factor specification called CMC (Common Mezzanine Card). The first two architectures to be ported to this mechanical form factor were SBus (SMC) and PCI (PMC). Up to this time, PCI boards (not counting PMC) were built with a .050" edge card connector for personal computer add-in cards.

The already enormous number of PCs with PCI slots and the low cost of the PCI interface chip ensure that there should be a continuous steam of PCI products for some time to come. The popular PCI products developed for the PC market will be natural candidates to be re-spun for other PCI form-factor implementations.

Today the following PCI applications exist or are being considered:

PCI on EISA-------Uses .050" edge card connector, exists on personal computer motherboards

PCI on ISA---------Uses .050" edge card connector, exists on personal computer motherboards

PCI on VME-------Uses 1mm blade-on-beam connector and CMC form factor, DEC, Motorola and Radstone have built product.

PCI on Futurebus--Uses 1 mm blade-on-beam connector and CMC form factor. No company is known to have built product at this time.

PCI on Multibus---Uses the CMC form factor. Intel just announced an 80486-based board with a PCI slot.

PCI on PCMCIA--Uses the high-density .8mm, two row, 100 contact, pin and socket PCMCIA connector. This is the standard PCMCIA connector available from Berg, Amp
Cannon, IBM and others.

PCI on CardBus---Uses a high-density pin and socket CardBus connector.

PICMG----------Uses the .050" PC style edge card connector on a passive backplane.

2mm PCI----------Proposed by Ziatec in conjunction with Zycom and Prologue as a passive, rack mount backplane with 2mm (IEEE 1301) connectors.

From the electrical side, the PCI architecture is implemented as a 33 MHz or 66 MHz, synchronous, unterminated, second incident bus. The 8 milliampere drivers will support 10 unit loads of capacitance with a connector pair being equal to one unit load and the PCI receiver being another unit load. Therefore, the PCI bus effectively will allow 5 devices to communicate with one device being the host system. From a software standpoint, the bus is hierarchical; supporting bus repeaters which allow the primary bus to support one or more secondary busses (possibly containing four more devices) and the secondary busses can support tertiary buses secondary to themselves. Its unterminated, short run (max. - 10 inches) nature make PCI an enabling, "driven" bus rather than a high performance system "driving" bus. The latencies inherent in the multiple hierarchies would severely limit its capability as a main system bus. However, PCI's high bandwidth of 132 Mbytes/second (32-bit transfers) or 264 Mbytes/second (64-bit transfers) is ideal for multimedia and embedded applications.

Digital, Intel, IBM, TI and others have built bus bridge chips, which allow a PCI bus to be extended. However, because the bus was designed as a local bus with no incident wave characteristics, no termination and no provisions for transmission line effects (only bulk capacitance) it may not be practical to extend the bus much more than 10 inches even with the bus bridge chips. All extensions naturally add latency to the bus structure and make peripherals at the end of the line less responsive.

PICMG is the PCI Industrial Manufacturer's Group, which is headquartered in Wakefield, MA. It is a trade consortium managed by Roger's Communication (617-224-1100). It represents the interests of Trenton Terminals, Ziatech, Technor, Texas Microsystems and I-Bus. Their interest is a passive, rackmount PCI implementation that will utilize the same edgecard connector that is presently used on the motherboards of personal computers, which support PCI function cards.

Hybricon has just started a PCI Passive Backplane Study Group within the VITA Standards Organization. This study group will define a PCI implementation on a Euro-card (IEEE 1101.1) mechanical form factor with a pin and socket connector for industrial applications where the industry standard PC style edgecard connector and PC form factor is not desirable. We will consider a PICMG proposal developed by Ziatech in cooperation with ProLog and Xycom as our first order of business. This proposal calls for a 7 row 2mm metric pin and socket connector. The PCI function cards will most likely be implemented on either a 3U-160 or 6U-160 card with the PCI connector in the lower 3U position.