Giving VME backplanes a shot in the arm

By Justin Moll

and Michael Munroe

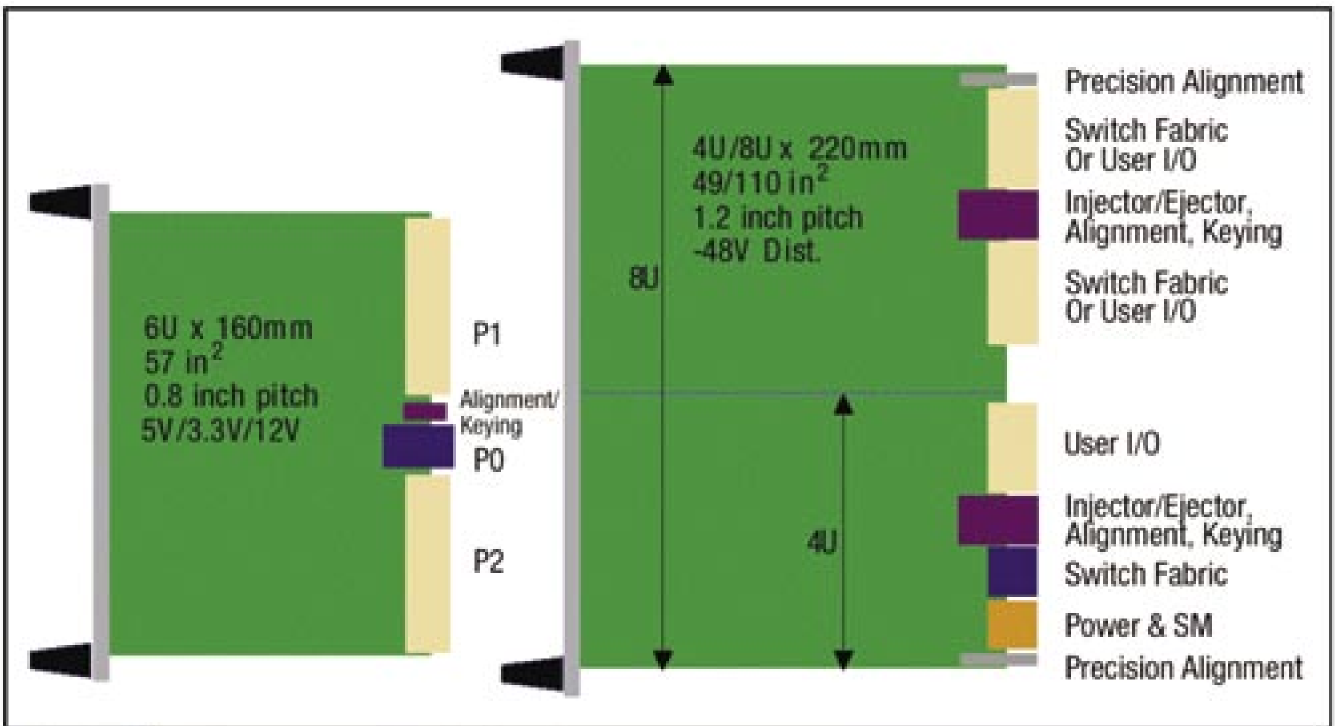
The demise of VME has been greatly exaggerated. Nearly every year we hear how VME is destined to fade away and at the 2004 Bus and Board conference, the talk in the halls proved that VME will again have to face the same questions. What is different this time around is that many of us in the VME community are starting to fight back. The battle is on two fronts: building awareness of VME's continuing advancement, and the new technological developments in VME that will take us to the next level. For technical advancements, there are many. The Motorola-led VME Renaissance and other VITA initiatives bring a wealth of new products and ideas for VME.

2eSST

You may have read of the new 2eSST technology that will bring standard VME backplanes from rough theoretical speeds of 80 MBps to 320 MBps. As the developers of the VME320 backplane (in 1997 in cooperation with Bustronic's consultant Drew Berding), we are particularly interested in how the new 2eSST-enabled boards perform in a VME320 system. We believe that the VME320 backplane would be a superior environment for the incident wave signaling capability of 2eSST drivers. Such an advantage might be of particular importance in very large systems where the combination of low voltage signals and background noise has created an adverse signaling environment. We are in discussions with other vendors in testing the results. But, the most promising of the next-generation VME backplanes appears to be the VXS Backplane (VITA 41).

VXS backplane

The VXS Backplane starts with a standard VME64x backplane design and implements a high speed fabric by replacing the existing P0 connector with a new high-speed MultiGig 7 Row connector and adding hub slots fully populated with the new connector. The new MultiGig connector and hub slots carry the high-speed switch fabrics, while the P1 and P2 connectors will support legacy VME64x cards (see Figure 1).



VITA 41 and VITA 34 form factor comparisons

Figure 1

This design maintains full backward compatibility while adding high-speed serial fabric connectivity. VITA 41 designers will have the flexibility of plugging in standard VME64x cards for parallel bus only, integrate VXS payload and switch cards for parallel bus and switch fabric transport, or use the VXS cards for switch fabric transport only. The current switched serial interconnects utilized are Infiniband and Rapid IO. In the future, other fabrics may also be implemented.

Design concepts for the VXS backplane

Accomplishing the dense routing on a 0.8-inch pitch with signals at 3.125 Gbps or higher in the VXS backplane requires some creativity. Even a mid-sized 12-slot Dual Star VXS backplane configuration (see Figure 2) forces the designer to make some difficult choices. One issue to avoid is letting the layer count get too high. The costs rise considerably, the backplane performance can suffer, and it prevents the use of available standard components (if the backplane is too thick, many standard connectors don't have long enough tails to fit through the board).

Another design concept is to avoid undesirable stubs for upper layer backplane traces. This presents two options. One choice would be to have these worst-case vias back-drilled – a costly fabrication process which removes the unused portion of the plated via structure below the layer at which the signal is terminated. The other choice is to minimize the length of via stubs by choosing a laminate with a lower dielectric constant. This will allow the 100-ohm differential impedance to be achieved with thinner PCB layers. A lower dielectric constant (E_r) is not the only characteristic that makes higher performance board materials attractive. High-grade materials such as Nelco 4000-13SI, Rogers 4350, and Mashusutta's Megtron 5 also have significantly lower loss tangent values at these higher frequencies. The loss tangent value indicates a degree of undesirable interaction with a signal at a given frequency. In the 12-slot Dual Star example, Bustronic chose to develop the backplane using Nelco 4000-13SI. The result is much improved signal integrity which provides better overall performance. This VXS backplane required 18 layers, a manageable and reasonable number for a high-performance backplane. For other future configurations (smaller slot counts, Single Star configurations, etc.) a standard FR-4 laminate may be sufficient, depending on the performance required.

As we demonstrated in previous AdvancedTCA papers, placing the hubs centrally for a VXS layout in most Dual Star configurations is a good choice. It reduces the maximum trace length, and there generally is a vast improvement in signal quality as the losses due to dielectric and skin-effect will be considerably smaller. Further, intelligent routing strategies can be implemented to minimize the layers count. Aside from lower PCB costs, having fewer layers minimizes the stub influence and improves the signal quality.

There are also other new specifications today and on the horizon for giving VME a boost in performance. The VITA 46 specification is being developed using many of the VITA 41 design concepts. VITA 46 appears to sacrifice backwards-compatibility for performance. One key goal is for more I/O signals. However, hybrid versions of either VITA 41 or 46 can have the backwards compatible VITA 41 payload slots with the 160-pin DIN connectors and slots on the side with all MultiGig connectors from top to bottom for more I/O and connectivity. We'll have to wait and see how the specification evolves. Other backplane-based VME technologies include VITA 31.1/31.2, and VITA 34.

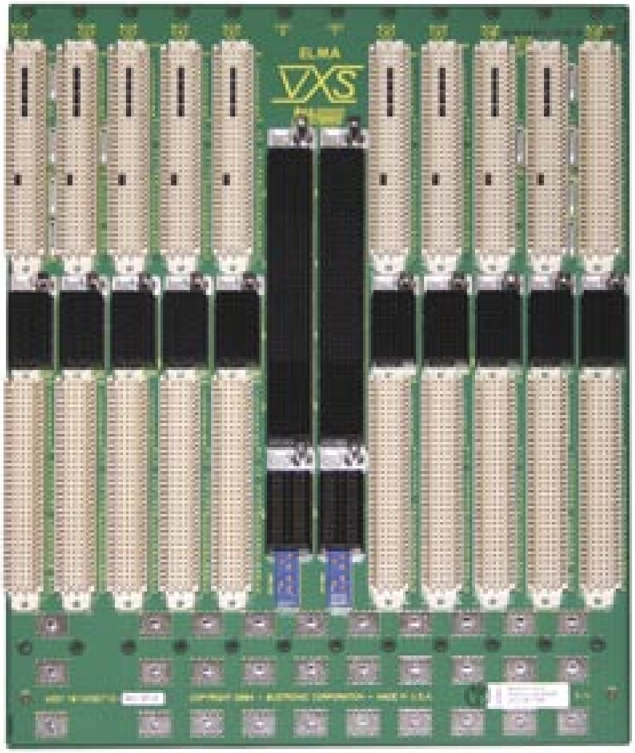


Figure 2

Gigabit Ethernet over VME (VITA 31.1)

The VITA 31.1 backplane is very similar in concept to the VXS backplane. However, it uses the standard 2mmHM connector in P0. There is full backwards-compatibility with VME64x cards with P0 connectors. However, you are limited to the performance of the 2mmHM connector. At least one company has developed node cards compliant to VITA 31.1, and a couple of backplane vendors have designs in the queue that are ready to go to fabrication when needed. A VITA 31.2 specification has been initiated for a StarFabric version.

Embedded modular (VITA 34)

VITA 34 is an aggressive and forward looking approach to mechanical packaging. In some ways similar to AdvancedTCA, it has a new form factor and may forgo the VMEbus altogether (see Figure 1). One of the standout features is the use of liquid cooling. The cards would be encased in metal, providing a cooling mechanical format for the cards and greatly improving shielding. Some in VITA feel that this will be critical as chip speeds increase where heat dissipation and shielding become much more important. The development for VITA 34 has not moved forward as quickly as hoped. However, no one doubts that new packaging technologies will be required for future systems. Bustronic is working with other VITA members to make sure that backplanes will be available to support our customers' needs for new mechanical and environmental packaging designs.

VME awareness

Fed up with hearing how the 25 year old bus which is still the most dominant player in standardized embedded systems is doomed, members of VITA gathered to discuss how to combat the industry's critical misperceptions of VME. The misperception that has been held for many years is that VME is dead, that the bus is too old and slow to keep up with today's computing needs. The truth is that VME has continued to expand and improve over time. From the 16-bit to 32-bit to 64-bit days, and from J1 VME to VME64x to VME320, the technology has progressed. Customers tell us that one of the great strengths of the VMEbus is that so many products are currently available for every potential application. We are working on innovative designs to ensure that that legacy boards will continue to be supported far into the future. The addition of a high speed P0 serial fabric will continue to breathe new life into the bus. The VME marketing committee has been formed to build awareness that VME continues to advance, strengthen the VME "brand," and develop more user-friendly tools for information on VME. Contact VITA for more details.

Simulation

Simulation is increasingly becoming a critical factor in high-performance backplane design. The fabrics used over VXS and VITA 34 will have speeds of up to 2.5 Gbps per port or higher, for a fabric channel bandwidth of 10 Gbps. Backplane designers will increasingly use simulation as part of their design for both standard products and custom designs. These models are increasingly being requested by SI engineers responsible for leading edge system design. Bustronic has developed our Signal Integrity Initiative (SII) to continuously enhance our backplane measurement and characterization program. Later in the year, Bustronic will provide new simulation data and models on various VXS backplane configurations, in addition to our data on AdvancedTCA backplanes.

Conclusion

The age of the VMEbus (and the corresponding VITA standards) creates a negative perception in the industry. However, it should also be recognized that the legacy of VME provides a stable, reliable, well understood technology with a wealth of vendors and product availability. Just as important, the industry should be aware that VME has evolved and improved over the years, and will continue to do so. With new standards that advance the technology like VITA 31, VITA 34, and VITA 41, the industry can look forward to advanced VME solutions for today and well into the future.

Justin Moll *has more than 10 years of high-tech marketing and sales experience and has been with Bustronic since 2000. As the director of marketing for Bustronic, he has led the company's charge in several next-generation technologies. Justin was recently re-elected as the VP of marketing for the StarFabric Trade Association. His previous positions include marketing services manager for E21 Corporation and account manager for Elcon Products International, now a Tyco Electronics company. Justin received his bachelor of science degree in business administration from the University of California, Riverside.*

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