VXS processor mesh: An ultrahigh-bandwidth configuration for VXS

By Michael Munroe

The VXS family of standards now defines an additional level of connectivity that can support the most demanding requirements and a wider selection of topologies than ever before. It accomplishes this feat without creating any new module or slot requirements and in a way that is fully compatible with existing VXS modules. This new implementation is being defined within VITA 41.7 and represents a significant enhancement of VXS flexibility and performance.

VITA 41.7 *VXS Processor Mesh* is a new configuration for VXS that offers tremendous bandwidth potential via mesh connectivity options. The newly proposed subsidiary specification, a *dot spec* of VITA 41, does not change the slot mechanics or fabric assignments of the new VXS *Payload* cards or the VXS *Switch* cards as they are defined in the base document, VITA 41.0.

However, a new backplane wiring scheme, VXS Processor Mesh, makes practical powerful new uses for VXS cards. In the process, it has transformed the common VME64x bus into possibly the fastest and most versatile architecture on the market today while doing nothing to interfere with the continued use of VME and VXS cards already on the market.That is: Backwards compatibility is maintained.

Adding mesh to VITA 41 VXS

To understand how Processor Mesh adds an important new capability to VXS, it's helpful to review the architecture and mechanics previously released as part of VITA 41.0 during the VME Renaissance effort at the Bus and Board conference in January 2003. The major performance leap of VXS is achieved by replacing the existing P0 connector with a higher speed and more rugged differential signal connector. This new MultiGigRT connector replaces the 2 mm HM connector that itself had only been added in 1997 and is an optional feature of VME64 extensions. The new VXS J0 connector carries two 10 Gbps fabric channels, as well as a collection of system management signals and some new reserved pins onto the 6U-160 backplane.

The 18 fabric A channels are routed through the backplane to a new fabric switch slot. A second identical slot is provided for the 18 fabric B channels. Each of the two fabric slots is populated from top to bottom with the new MultiGigRT differential connectors. These two new types of slots, payload and fabric, are the extent of the mechanical and connector changes that are defined by VITA 41.0.

The new P0 connectors and the fabric slots can be identified by their black color, and the new VXS guide pins can be seen in Figure 1. This 12-slot VITA 41.7 backplane from Elma Bustronic provides five meshed processor slots. It also includes two legacy VME64x slots and only requires a single switch card to support both center fabrics. From an electrical perspective, it will not be difficult to migrate the traditional P0 functions such as GbE, Myrinet, and other I/O signals out the backplane, to the new MultiGig J0/P0.

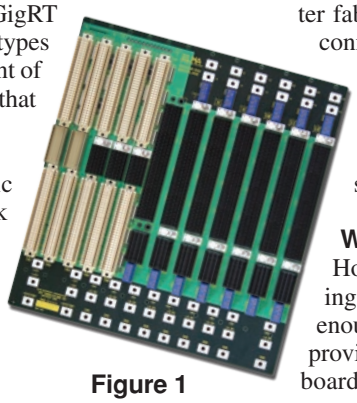

Figure 1

> "... VXS Processor Mesh...has transformed the common VME64x bus into possibly the fastest and most versatile architecture on the market today..."

Architecture choices

The new fabric slots as defined originally in VITA 41.0 (VXS Core Standard) actually supports two very different architectures. The first and immediately obvious architecture is a dual star topology with two high-speed channels, allowing a private communication path between any two payload cards. These transient connections are provided as needed by either of two switch cards to which each payload card is connected (Figure 2). VITA 41.7 brings together four primary buses: VME64x, VXS center fabric, IPMB, and Processor Mesh.

The second type of system architecture and possibly the most popular is not directly described within VITA 41.0 but is supported perfectly.

If processing cards are installed in the two fabric switch slots, a point-to-point topology is established between payload and switch slots. In this case, the payload cards are not using the center fabric to link to other payload cards but instead as a direct connection to resources in the switch or hub location.

Today up to five FPGAs or other specialized processing engines can fit onto a single 6U-160 switch card. The signal processing power possible with two such cards is substantial and more than sufficient for most applications.

When *more* isn't enough

However, there remain applications – such as image processing or complex computational tasks – where two cards are not enough. For this sort of requirement, VXS Processor Mesh now provides a fully meshed network of up to five switch slots. Each board is connected to every other board by four 16x channels

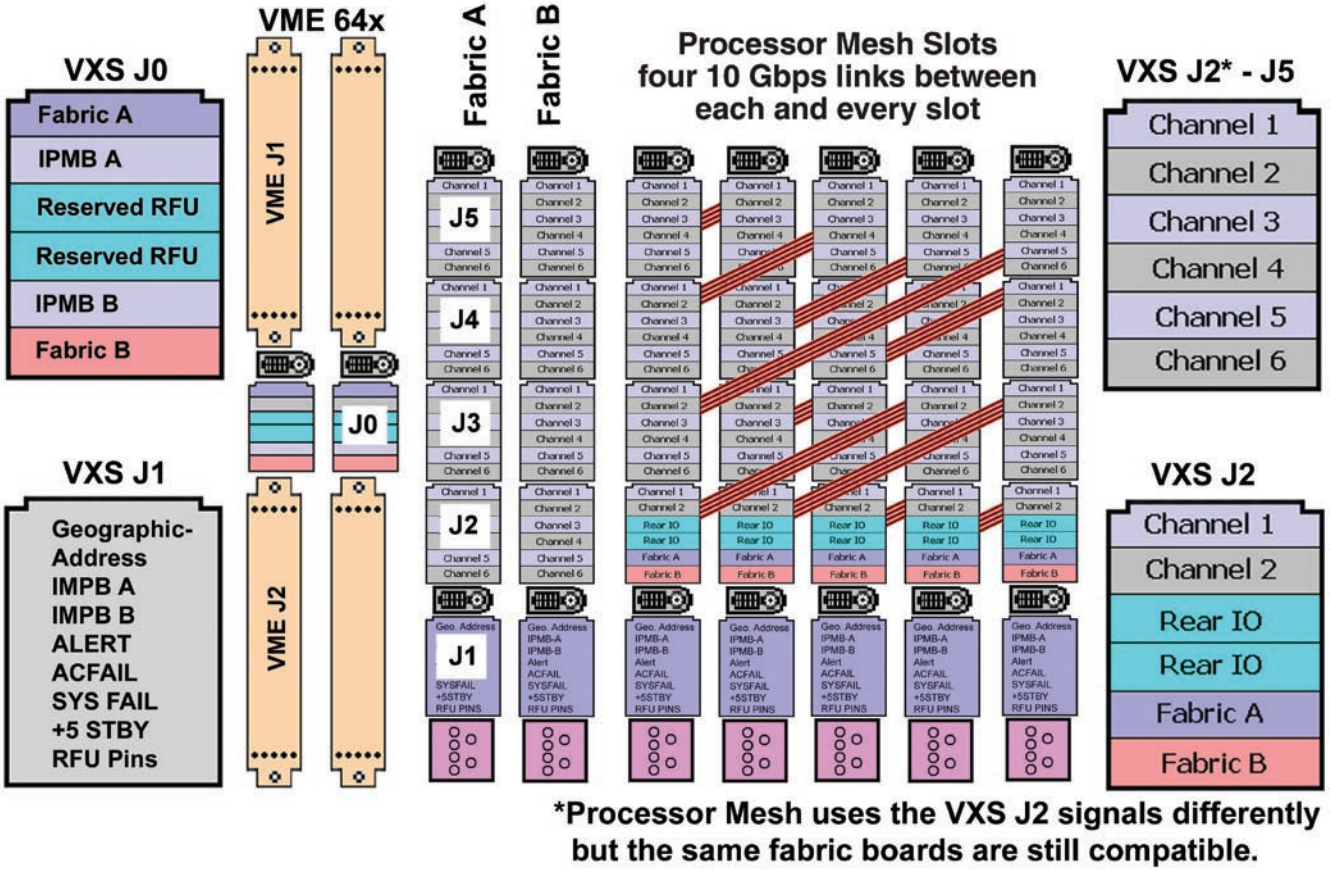

Figure 2

as can be seen in Figure 3. In this instance, Processor Mesh can support pipelines, rings, stars, and meshes with one backplane. In each of those topologies, there are four full 4x channels between each and every module. Multiple five-slot Processor Mesh segments are possible in a single backplane.

Processor Mesh can be ideal for many diverse processing tasks because it supports a wide range of system topologies including distributed processing, pipeline processing, signal switching, star architectures, and rings. The four-channel redundancy offers (at today's speeds) a 40 Gbps path and as signaling technology scales, the bandwidth of this mesh should never be a limitation.

Built into the specs

The VITA 41.0 base document specifies other important features such as an Integrated Platform Management Bus (IPMB). This I2C bus is implemented on the center connector of each payload connector. Two signals are named, PA_SCL and PA_SDA. To support a second redundant management controller, a second duplicate set of signals is also provided: PB_SCL and PB_SDA. These signals are all routed from the payload J0 connector to the connector J1 in both fabric slots.

A new VXS subspecification called *VITA 41.6* proposes using these J1 signals to implement a separate control plane. This specification utilizes existing point-to-point links that originate in the J1 connector of the switch slot and connect to the J0 connector in each payload slot for a wide variety of system functions such as board reconfiguration, launching applications, cluster management, remote management, or e-keying. E-keying is a configuration process by which a card provides specific information about itself such as ID, functionality, and power requirements when interrogated by the system manager. The fixed slot defini-

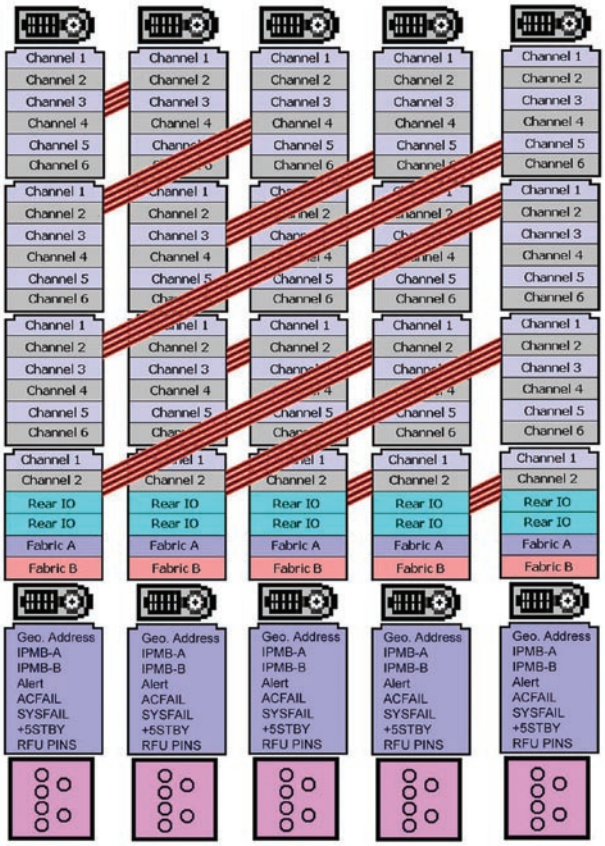

Figure 3

tions of VXS and Processor Mesh ensure multivendor interoperability, which supports a stable and secure ecosystem.

When introduced, VXS supported legacy VME64x while providing new system management signals and more power. While standard VXS initially added two 10 Gb central fabric channels in a dual star topology, VXS Processor Mesh goes far beyond. Processor Mesh adds a special bus segment supporting five highly connected fabric slots for processing cards. By maintaining a tight integration with legacy VME64x cards, VXS preserves the value of existing hardware, and together with Processor Mesh creates a flexible architecture with a fabric connectivity rivaling the fastest backplane topology proposed by any new architecture to date.Ω

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